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13. ABSTRACT (Maximum 200 words)

This program carried out an evaluation of optical transmitter and receiver technologies for parallel data processing applications. The system performance has been evaluated in terms of the maximum interconnect density at a given data rate. A new III-V smart pixels technology that monolithically integrates MODFETS with MQW modulators and detectors operating at 1064nm wavelength has been developed to fully exploit the high speed of optoelectronic devices while keeping compatibility with flip-chip bonding to silicon chips. A complete characterization of this monolithic III-V smart pixel technology has been carried out, including the S-and Y- parameters extraction for the typical devices implemented by this technology. To demonstrate the applicability of this technology we have implemented a transimmpemdance receiver circuit with bandwidth of 9 GHz and an 8x8 active-pixel sensor array with 285 MHz operation.

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Smart pixel technologies for interfacing optical memories with optoelectronic computing systems and guided wave optical interconnections

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1. *Objectives and Accomplishments*

The main objective of this program was the investigation of the potential application of the smart-pixel technologies to interface parallel optical memory and computing systems. In this program, we have carried out an evaluation of optical transmitter and receiver technologies for parallel data processing applications. The system performance has been evaluated in terms of the maximum interconnect density at a given data rate. A new III-V smart pixels technology that monolithically integrates MODFETS with MQW modulators and detectors operating at 1064nm wavelengthhas been developed to fully exploit the high speed of optoelectronic devices while keeping compatibility with flip-chip bonding to silicon chips. A complete characterization of this monolithic III-V smart pixel technology has been carried out, including the S- and Y-parameters extraction for the typical devices implemented by this technology. To demonstrate the applicability of this technology we have implemented a transimpemdance receiver circuit with bandwidth of 9 GHz and an 8x8 active-pixel sensor array with 285 MHz operation.

2. *Optoelectronic technology evaluation*

In the design of a massively parallel optoelectronic system for optical memory interface, one of the considerations is the maximum interconnect density. The interconnect density at a given bit rate determines the aggregate bandwidth or the data transfer rate from the storage system. Because optoelectronic devices and circuits dissipate significantly more power on chip comparing to CMOS logic circuits, the maximum power dissipation limits the maximum interconnect density in a parallel optoelectronic system. We have developed a method of minimizing the total power dissipation of an interconnect link at a given bit rate. The performance of two transmitter technologies, VCSELs and MQW modulators and their associated driver-receiver circuits including CMOS and bipolar transmitter driver circuits, and PN photodetectors with multistage transimpedance receiver circuits have been examined.

2.1 Interconnect model

A FSOI link begins at the input of the transmitter driver circuit and ends at the output of the receiver decision circuit. The input digital electrical signal is first fed into the transmitter driver circuit, converted to an optical signal by the transmitter, and then routed to the detector by the optical system. The detected signal at the detector is converted from a photocurrent to an analog voltage and amplified by the receiver amplifier. Finally, the receiver decision circuit outputs a digital logic level by applying a threshold to the received analog signal.

Our optimization goal is to choose the link design that minimizes the total on-chip electrical power dissipation of the link for a maximum operating bit rate. We define the maximum operating bit rate of a given FSOI link as the bit rate beyond which the reliability of communication drops below a specified BER, as determined from the rise-

time of the signal at the decision circuit's input. Thus the maximum operating bit rate includes the rise-time of the transmitter and of the receiver circuits.

2.2 Transmitters

We have analyzed MQW modulators and VCSELs with their driver circuits. CMOS circuits are examined for driving both MQW modulators and VCSELs. Bipolar transistors are studied to drive VCSELs for high bandwidth applications.

2.2.1. MQW Modulators with CMOS Driver Circuits

Figure 1 shows the circuit schematic of a MQW modulator driven by a CMOS superbuffer circuit. The superbuffer is a set of cascaded inverters, and the size of each inverter is larger than the previous one by a constant factor of β. The value of β is chosen typically between 3 and 4 to minimize the overall propagation delay of the superbuffer and is determined from the parameters of a minimum size transistor for a given CMOS technology. The first inverter is a minimum size inverter, and the last inverter drives the modulator.

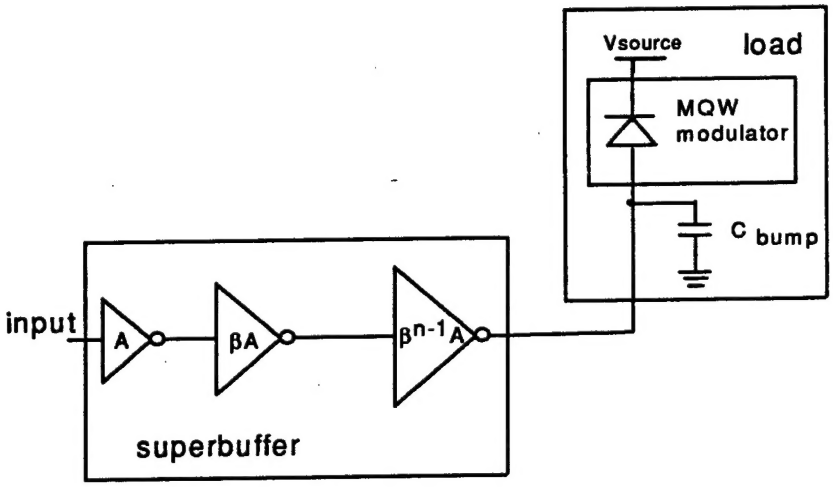


Figure 1 CMOS superbuffer driving the MQW modulator

The total power dissipated in a superbuffer is given as

$$P_{sb} = C_{total} \cdot V_{dd}^2 \cdot \frac{BR}{2} \qquad (1)$$

where C_{total} is the total capacitance of the superbuffer including the modulator capacitance and any parasitic capacitance as seen by the last inverter of superbuffer. BR is the bit rate with units of bits/second.

In most cases, the modulator capacitance is small enough (~ 10 fF) that a single inverter is sufficient to drive the modulator. However, a larger superbuffer with more inverters can be used to reduce the rise-time of the output optical signal, provided the

total propagation delay of the superbuffer does not exceed the bit period. The fast rise time in turn reduces the power dissipation in the receiver. The cost is, however, the additional electrical power dissipation of the superbuffer circuit. In our analysis, the optimum number of superbuffer stages is determined by balancing the power dissipated in the superbuffer stages and in the receiver circuit such that the total power dissipation is minimum at any given bit rate.

The minimum MQW modulator area used is 10 μm x 10 μm with a capacitance of 0.1 fF/μm^2. The saturation intensity is assumed to be 10 kW/cm^2. The modulator area is enlarged when the input optical intensity exceeds the saturation limit. The modulator performance is characterized by its contrast ratio (CR) and insertion loss (IL) at its optimal bias voltage (V_{bias}) with a voltage swing (ΔV). The maximum voltage swing is determined by the voltage supply of the driver circuit (V_{dd}). The power dissipation in the modulator due to absorbed light power is derived in Appendix A as

$$P_{diss,MQW} = \frac{F \cdot P_{opt,rec}}{\eta_{link}} \cdot \frac{q}{h\nu} \cdot \left(\frac{V_{bias} \cdot \left(1 + IL - \frac{1-IL}{CR}\right) - V_{dd} \cdot IL}{(1-IL) \cdot \left(1 - \frac{1}{CR}\right)} \right) \qquad (2)$$

where $P_{opt,rec}$ is the average optical power required at the receiver input, F is the system fan-out, and η_{link} is the optical system efficiency. The total power dissipation of the transmitter is the sum of the power dissipated in the modulator due to optical absorption described by Eq. (2) and the switching power of the superbuffer described by Eq. (1). The optical power in a modulator based system is generated by an external light source, and the electrical power dissipation of the light source is thus not included in the total on-chip power dissipation.

2.2.2 VCSELs with Driver Circuits

A typical laser driver circuit consists of impedance matching circuitry at the input and the output, an adaptive stage, and an output driving stage. The adaptive stage includes logic circuits to reduce the overall power consumption, shift the levels of various signals, compensate for current variations, eliminate jitter, and/or to equalize the rise and fall times. The output driving stage provides the current (the threshold as well as the modulation currents) to the laser. The load consists of the laser diode and a parasitic capacitance. Usually the power dissipated in the last output stage is much greater than that in all other auxiliary circuits. Thus, we consider only the output stage.

The output stage of the CMOS VCSEL driver circuit (Figure 2) consists of two NMOS transistors (N_B and N_A) providing the threshold and the modulation currents, respectively, and a superbuffer driving the gate of N_A. The superbuffer is implemented in the same manner as described in Section 2.2.1.

The total electrical power dissipated in the driver and VCSEL can be separated into two parts: the power dissipation of the superbuffer given by Eq. (1), and the power dissipation of the VCSEL and the two transistors due to their current flow. The bias transistor (N_c) can be shared by multiple drivers - its power dissipation is thus neglected in the single link calculation. The total laser current (I_{total}) is the sum of the threshold current (I_{th}) and the average modulation current (I_m). The modulation current is assumed to have a 50% duty cycle. The source voltage (V_{source}) is the sum of the threshold voltage

of the VCSEL (V_{th}), the voltage drop across its series resistance (R_s) when the modulation current flows, and the minimum source-drain voltage (V_{dd}-V_{tn}) required to ensure that the transistor N_A is in its saturation region. The total electrical power consumed in the VCSEL and the output stage is then

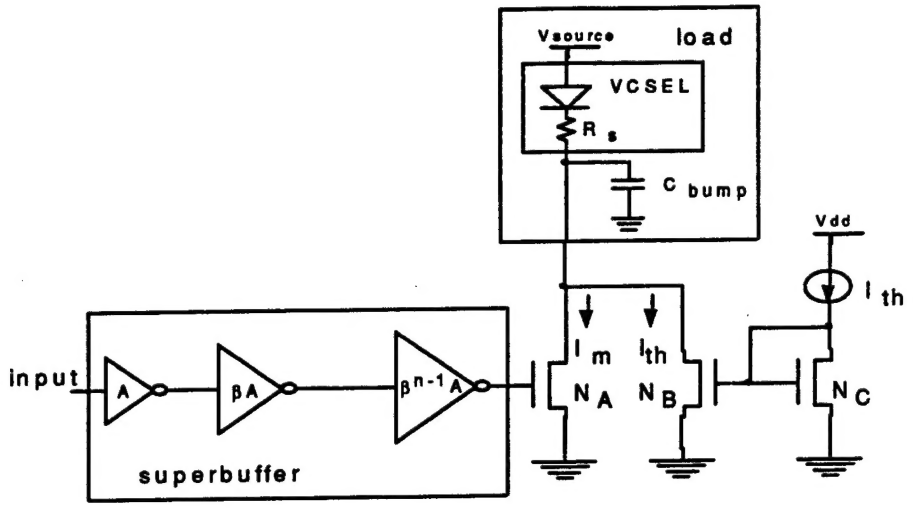


Figure 2. Output driving stage of a CMOS driver connected to the VCSEL

$$P_{CMOS,VCSEL} = I_{total} \cdot V_{source} = \left[I_{th} + \frac{I_m}{2} \right] \cdot \left[V_{th} + R_s \cdot I_m + (V_{dd} - V_{tn}) \right]. \quad (3)$$

For a given laser slope efficiency (η_{LI}), the average output optical power is

$$P_{opt,transmitter} = \frac{I_m \cdot \eta_{LI}}{2}, \quad (4)$$

where the spontaneously emitted power at threshold is neglected. The total power dissipated in the transmitter circuit ($P_{transmitter}$) is then the sum of Eq. (1) and (4) minus the laser output from Eq. (5). From Eq. (4) one can see that the last term in the second parenthesis, (V_{dd}-V_{tn}), is solely from the driver circuit. The power dissipated in the driver circuit is about the same as in the VCSEL itself using 0.5 μm CMOS technology. Therefore, the power conversion efficiency, including the power dissipation of the driver circuit, reduces by about 50% compared to that when considering the VCSEL alone.

The output driving stage implemented using bipolar transistors is shown in Figure 3. Due to parameter variations in bipolar technology, a differential configuration is necessary. The sum of the emitter currents of transistors Q_B and Q_A is fixed by connecting a current source to the transistor Q_C. The partitioning of this fixed current between Q_B and Q_A depends on the differential voltage supplied to the bases of these two transistors. The currents in these transistors are designed such that when the threshold current (I_{th}) is flowing through Q_B, the current through Q_A is equal to I_{th} plus I_m, and vice versa. The total current in the output driving stage is thus ($2\,I_{th} + I_m$). The power supply voltage for the bipolar driver is the sum of the threshold voltage, the voltage drop across its series resistance, and the collector-emitter voltage (V_{ce}) across both Q_B and Q_C. For a high frequency operation, both Q_B and Q_A are always biased in their active regions. V_{ce} is

typically 1V or higher when a BJT is in its active region. The total dissipated power is then

$$P_{bipolar,VCSEL} = [2 \cdot I_{th} + I_m][V_{th} + R_S \cdot I_m + 2V_{ce}] \quad (5)$$

which is about twice as that in a CMOS driver.

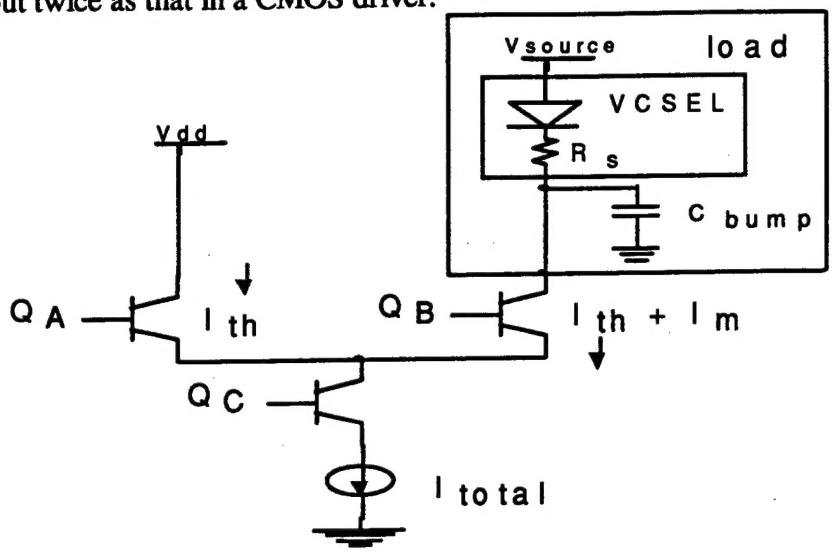


Figure 3 Output driving stage of a bipolar driver connected to the VCSEL

2.3 Receivers

In this analysis, the receivers considered are solely of the transimpedance type due to their high bandwidth, low noise, and ease of biasing. The operational model of a transimpedance receiver can be broken into four components (Figure 4) - the detector, the transimpedance amplifier, the voltage amplifier, and the decision circuit. The detector produces the photo-current based on an optical signal. The transimpedance amplifier converts the photo-current from the detector to an analog voltage. This voltage is then amplified by the voltage amplifier to match the input requirements of the decision circuit. The decision circuit provides a digital voltage output to the following computational logic circuits.

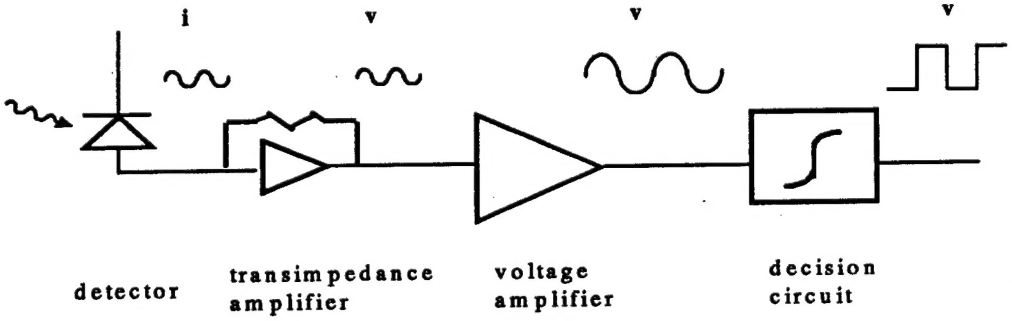


Figure 4 Block diagram of a receiver

The receiver designs considered are based on CMOS current-source inverters. For a given CMOS technology, the design of the receiver gives the receiver rise/fall time (tr_{rec}), the required average optical power at the detector ($P_{opt,rec}$), and the electrical power dissipation in the receiver ($P_{elec,rec}$). The design parameters are the number of stages in the transimpedance amplifier (s) and in the voltage amplifier (p) and the widths and bias gate-source voltages (w and v) of the amplifying transistors.

The maximum bit rate of the receiver can be determined by placing requirements on the pulse shape of the output signal. The rise/fall time of the output pulse is set to be a certain fraction (ζ) of the bit period to ensure a reasonable bit error rate. A typical value for ζ found in the literature is about 60%. The maximum bit rate can then be written as

$$BR = \frac{\zeta}{\sqrt{tr_{in}^2 + tr_{rec}(s,p,w,v)^2}} \qquad (6),$$

where tr_{in} is the rise time of the optical input signal (as determined by the transmitter driver), and tr_{rec} is the rise time of the receiver amplifiers and is a function of the design parameters mentioned above.

The average optical power swing required at the detector is given by

$$P_{opt} = \frac{V_{dd}}{2 \cdot A_{dc} \cdot R_{pd} \cdot [A_v(w,v)]^p \cdot Z_f(s,w,v)} \qquad (7)$$

where A_{dc} is the gain of the decision circuit, R_{pd} is the responsivity of the detector, A_v is the gain of the voltage amplification stages, and Z_f is the transimpedance of the transimpedance amplifier. The transimpedance is determined by finding the feedback resistor that gives a maximally flat magnitude response from the transimpedance amplifier. The required optical power at the detector is related to the optical power output from the transmitter by an efficiency (η_{link}) of the optical system between them and the transmitter fan-out (F), *i.e.* $F\,P_{opt,rec} = \eta_{link}\,P_{opt,transmitter}$.

The electrical power dissipated in the receiver is

$$P_{elec,rec} = (s+p) \cdot I_{ds}(w,v) \cdot V_{dd} \qquad (8)$$

where I_{ds} is the bias current and depends on the parameters w and v. Thus, the number of stages in the amplifiers, and the width and bias voltage of the amplifying transistors determine the optical power requirement and power dissipation of the receiver. The bit rate of the receiver, however, is not only determined from these parameters; it is also a function of the rise time of the input optical signal.

In addition to the power dissipation described by Eq. (8), the power due to the absorbed photocurrent is another component in the total receiver power dissipation

$$P_{rec,abs} = P_{opt,rec} \cdot \frac{q}{h\nu} \cdot V_{bias} \cdot \frac{CR+1}{CR-1} \qquad (10)$$

where V_{bias} is the bias voltage of the detector which is set equal to V_{dd}, and CR is the contrast ratio of the input optical signal. When the VCSEL is biased at threshold, CR is assumed to be infinite.

2.4 Optimization methodology

Our optimization methodology takes the link design parameters and constraints as input, and iterates over the design variables to find the optimum link design for a given bit rate. The link is characterized by five sets of parameters: the characteristics of the CMOS (or bipolar) technology used, the transmitter characteristics, the optical system efficiency, the system fan-out, and the receiver characteristics. In addition, there is a set of constraints including the stability of the receiver (i.e. its transfer function approximates a maximally-flat magnitude response), and that the propagation delay through the transmitter driver must not exceed the bit period of the link. For a given set of transmitter characteristics, the optimized design variables are the number of stages in the transmitter driver, the number of stages in the receiver, the value of the feedback resistor in the receiver, and the transistor width and bias voltage in the receiver gain stages.

In the iteration process, we first choose values for the receiver variables that meet the constraint of a stable receiver response. This determines the required optical power at the detector, which is then translated to a required output optical power from the transmitter, taking into account the optical system efficiency and the fan-out. We then vary the number of stages in the transmitter driver, while ensuring the propagation delay through the transmitter driver does not exceed the bit period of the link. More stages in the transmitter driver results in a shorter rise time of the output optical signal, thus a higher maximum operating bit rate. However, these extra stages increase the power dissipation in the transmitter circuit. We record the maximum operating bit rate and the power dissipation for each set of variables that meet the design constraints. The optimum designs are the ones resulting in the minimum power dissipation at a given operating bit rate.

Using this method, we evaluated reflection-mode modulator, ASFP-MQW modulator, ion-implanted VCSEL, and oxide-aperture VCSEL technologies. Figure 5 shows the minimum power dissipation per link when the driver and the receiver circuits are implemented in 0.5 μm CMOS technology and Figure 6 show it when using 0.1 μm CMOS. The interconnect densities are indicated on the right vertical axises using the maximum heat dissipation density of 10 W/cm^2 in air-cooled silicon. Figure 7 is a comparison of the link power dissipation of the two VCSEL structures when their driver circuits are implemented using CMOS and bipolar technologies. The effect of the system fan-out is shown in Figure 8.

The results from the devices and technologies chosen show that with recent developments in VCSEL technology, namely oxide-aperture devices, using VCSELs as transmitters in optoelectronic systems offers comparable interconnect densities with MQW modulators (based on their power dissipation) at high bit rates – above 800 Mbits/sec with 0.5 μm CMOS driver circuits and 1.5 Gbits/sec with 0.1 μm CMOS driver circuits. Even with low threshold-current oxide-VCSELs, the VCSEL based systems still pay a considerable power penalty due to the threshold. This penalty becomes less significant when VCSELs are used in applications requiring larger fan-outs and/or higher bit rates, where the modulation current dominates the threshold current of the VCSEL. In these applications, VCSELs with a high slope efficiency are suited than those with a low threshold current. There is a 50% improvement in the maximum operating bandwidth

when scaling the CMOS technology from 0.5 μm down to 0.1 μm since the gain-bandwidth product of the receivers is increased.

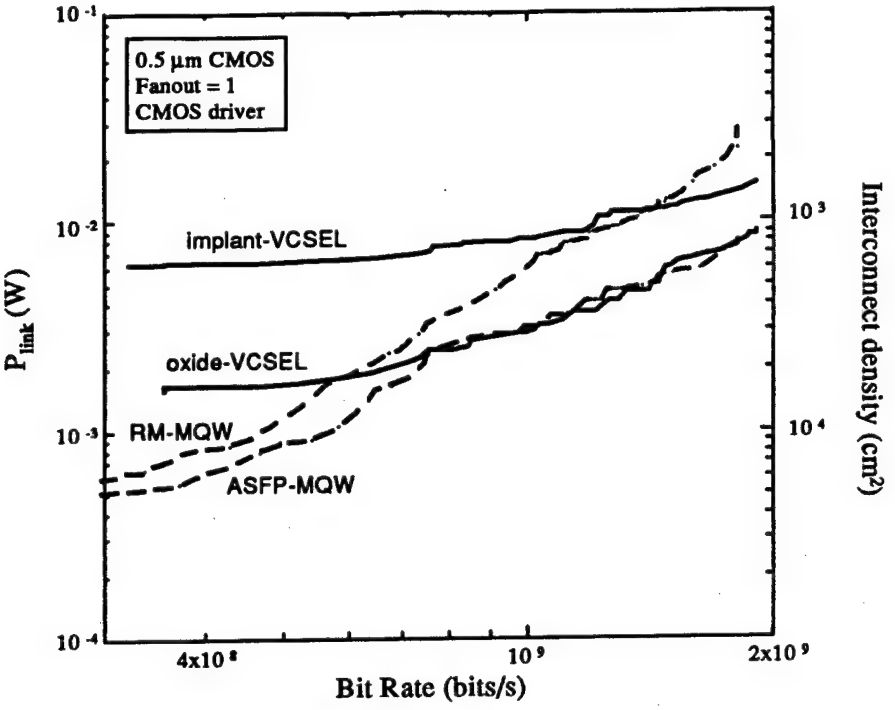


Figure 5 Minimum power dissipation per link vs. bit rate for MQW and VCSEL transmitters

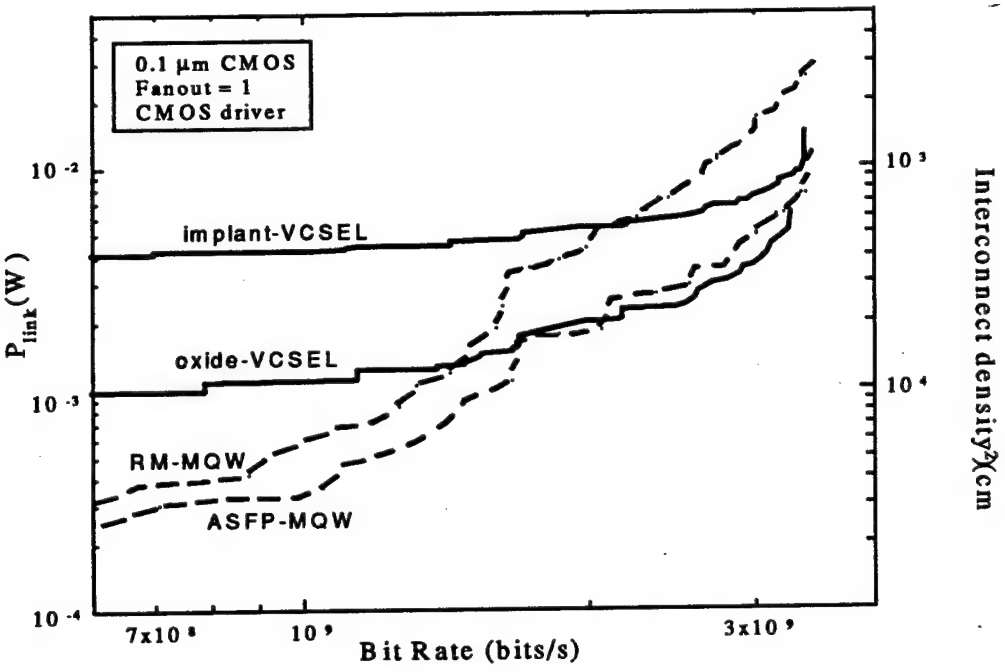


Figure 6 Minimum power dissipation per link vs. bit rate for 0.1 μm CMOS technology

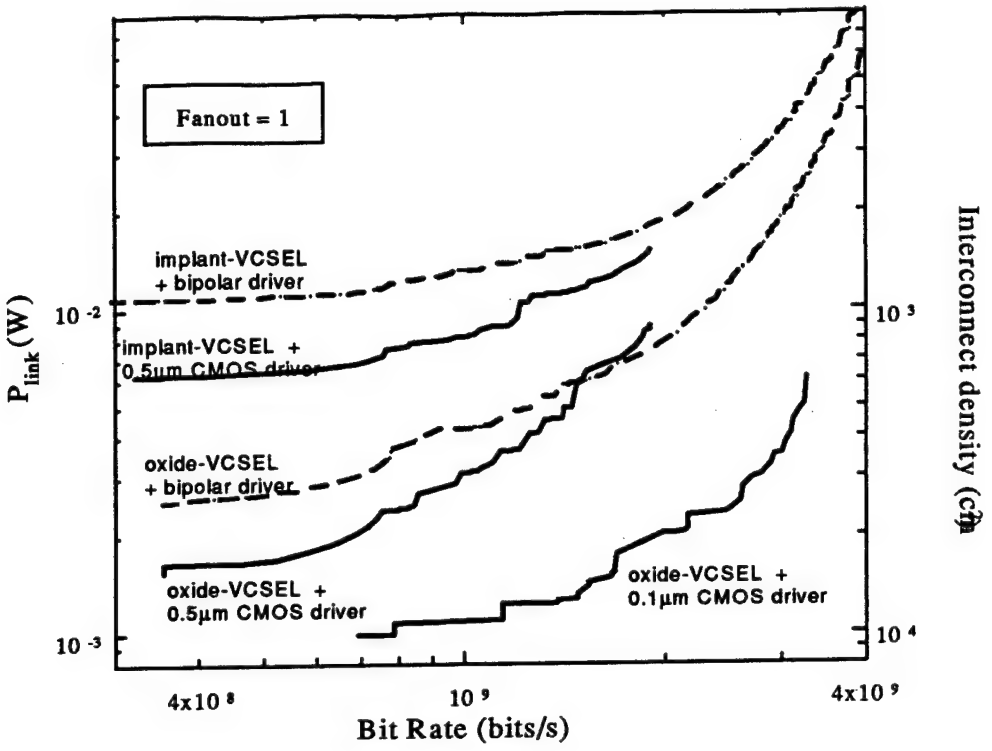


Figure 7 Minimum power dissipation per link vs. bit rate for VCSEL based links with CMOS and bipolar drivers

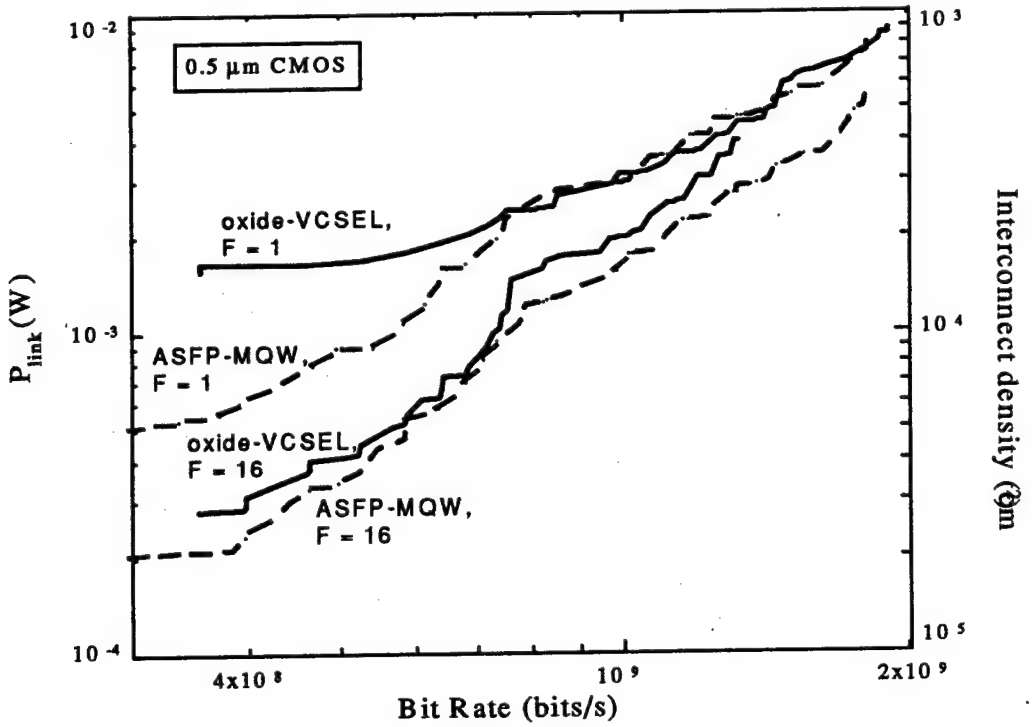


Figure 8 Minimum power dissipation per link vs. bit rate for different fan-out

The transmitter driver circuit is an important component in the link design. The electrical power dissipated in the CMOS driver circuit is about the same as that in the VCSEL itself, which reduces the total power conversion efficiency by 50%. Other techniques can be investigated to reduce the modulation current required at the transmitter VCSEL (e.g. VCSEL based pre-amplifiers, GaAs based receivers, etc.). These techniques are expected to reduce the overall link power, and can be incorporated into the design methodology presented in this paper.

In the optimized links, the power dissipated in the transmitter unit dominates that in the receiver circuit, except when MQW modulators are used as the transmitters at low bit rates. More sensitive receiver circuits can be designed in applications where the power dissipation in transmitter circuits needs to be minimized. The total power dissipation of the link in the later case, however, will be higher than that of the optimized design.

With either VCSELs or MQW modulators, an aggregate bandwidth in excess of 1 Tbits/sec-cm^2 can be achieved in an optimized free-space optical interconnect system.

3. Monolithic integration of III-V OE circuits

The monolithic integration technique to implement high speed smart pixels we developed is based on InAlGaAs/InGaAs MQW materials on GaAs substrates. The objective of the work was to develop small-scale integration of high-speed III-V optoelectronic devices and then flip-chip bond them to silicon-VLSI circuits. Applications of this approach include low-noise optical receivers and high-frequency serial-to-parallel signal converters such as required in optical memory interfaces..

The electro-optical devices integrated are InAlGaAs/InGaAs MQW light modulators operating around 1.06 μm wavelength. Since GaAs substrates are transparent at this wavelength, the integrated III-V circuits can be flip-chip bonded to silicon VLSI chips without removing the GaAs substrate. However, there is about a 2% lattice mismatch between the InAlGaAs/InGaAs MQWs and the GaAs substrate. Through the insertion of compositionally step-graded InAlGaAs buffer layers with increasing indium composition[1], we are able to grow quality InAlGaAs/InGaAs material reproducibly on GaAs substrates with a limited dislocation density. In this material system, we are also able to use InGaAs with high indium content in the FET channel to enhance the electronic device performance.

3.1 Material layer structure and DC characteristics

The typical material layer structure for the integrated MODFET on top of the MQWs is shown below (Figure 9). It is designed such that a modulation-doped FET channel is inserted into the n-contact layer of a MQW PIN device; it permits the fabrication of both devices from the same epitaxial layers. Both enhancement-mode and depletion-mode MODFETs have been fabricated using the same epitaxial layers. The use of enhancement-mode and depletion-mode devices allows the design of low-power logic circuits for optoelectronic applications.

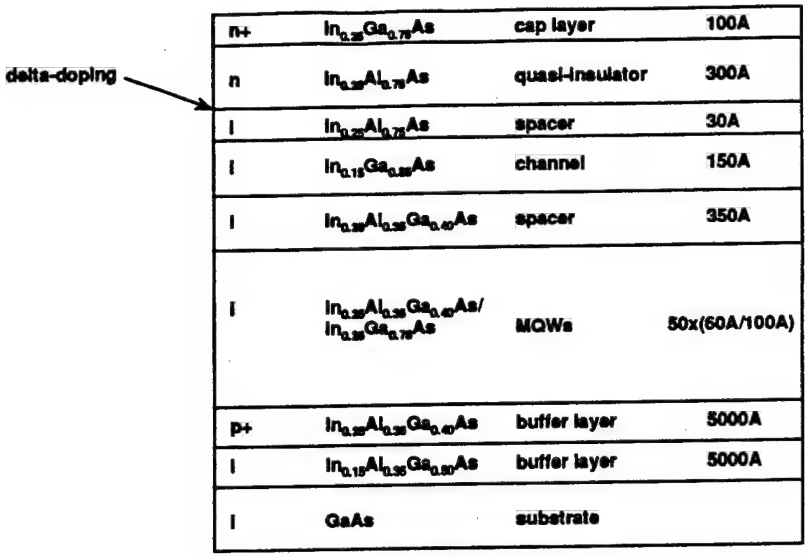


Figure 9 Layer structure for an integrated MODFET and MQW pin modulator/detector

DC and S-parameter measurements were made on different sized enhancement and depletion mode FET structures. The S-parameters were measured at various bias points across the different regions of operation for the FETs from 0.5 to 26 GHz. The DC measurements included I-V, gate current and g_m measurements. Figure 10 and 11 show the measured DC characteristics for a double heterostructure silicon delta-doped InAlAs/InGaAs pseudomorphic HEMTs. Fairly large transconductance near 400 mS/mm were measured for the enhancement-mode devices and over 300 mS/mm for the depletion-mode devices. The maximum current density was approximately 300 mA/mm for the device.

One of the concerns in III-V MESFET and MODFET technology is the gate leakage which occur under reverse and forward bias conditions. With the use of the large bandgap quasi-insulator $In_{0.25}Al_{0.75}As$ these effects are significantly reduced. For some of the enhancement-mode $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFETs, gate-source voltages of up to 1.25 V could be applied without significant gate leakage. In addition, excellent reverse gate drain diode characteristics were measured and are plotted in Figure 12. The gate drain breakdown was over 20 V if one specifies the breakdown current density to be 10 μA/μm.

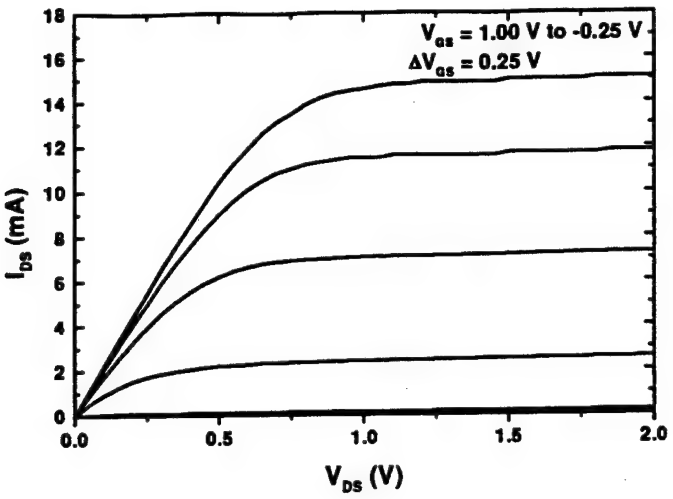


Figure 10 Drain I-V characteristics for a 1.0x50 μm^2 enhancement-mode $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFET

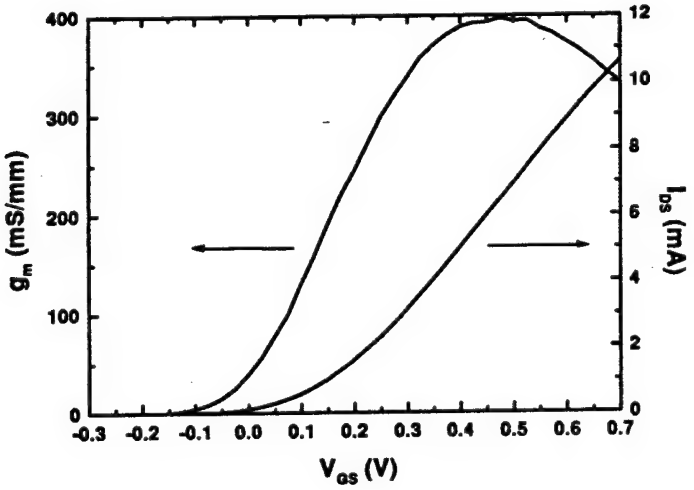


Figure 11 g_m and I_{DS} as functions of V_{GS} for a 1.0 x 50 um^2 $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFET

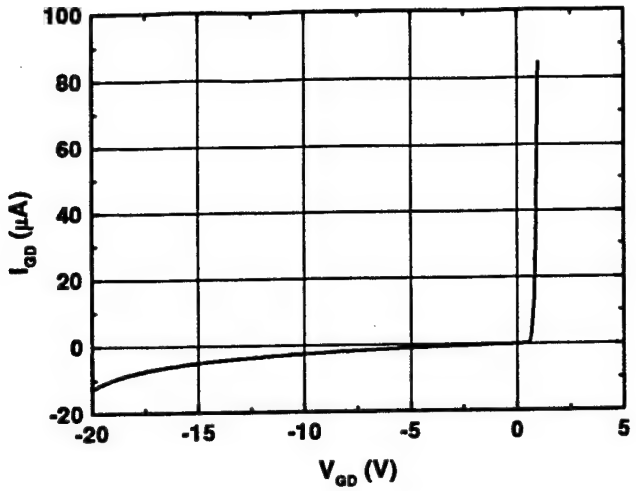


Figure 12 I_{GD} as functions of V_{GD} for a 1.0 x 50 um^2 $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFET

3.2 RF parameter extraction

3.2.1 MODFETs

Many different small-signal circuit topologies can be used for modeling the properties of FETs. Though the extrinsic parasitic elements may slightly differ in their placement in the equivalent circuit, the intrinsic transistor model is usually the same. The general description of the small circuit equivalent circuit is shown in Figure 13. An unique feature of the material layer structure used in this technology is that there is an underlying p-layer to raise the electron potential from the substrate side so that the electrons are confined in the channel region. To account for this feature, the drain-source capacitor (C_{DS}) is modified by that shown in Figure 14.

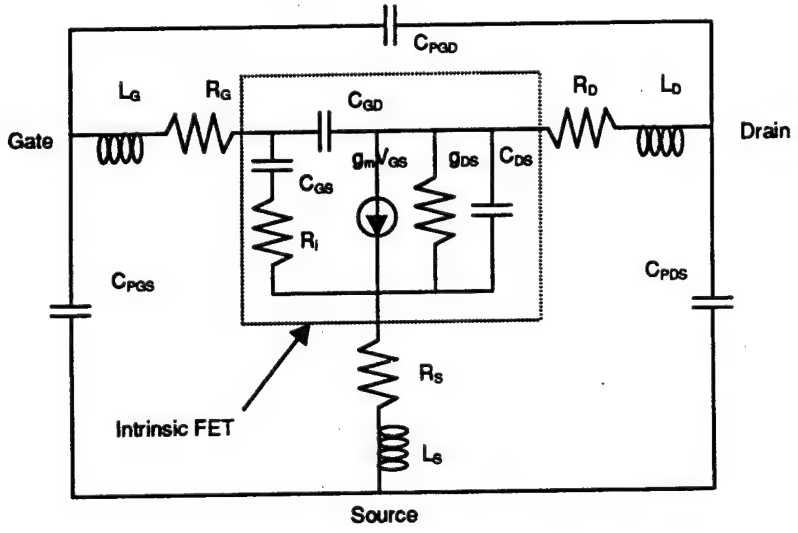


Figure 13 Equivalent circuit representation of a FET

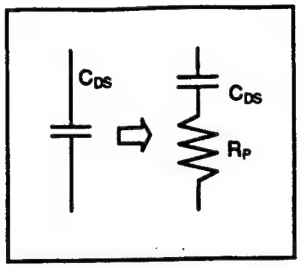


Figure 14 Modified small signal representation to account for underlying p-layer

The extrinsic elements were first determined by using transmission line model for the resistances and inductances and pinched the FET method for capacitances. The results are summarized in Table 1. S-parameter measurements and curve fitting then determined the intrinsic parameters. Table 2 summarizes the intrinsic parameters and Figure 15 includes the s11 and s22 smith chart.

Table 1 Summary of extrinsic parameters

L_G (nH)	L_D (nH)	L_S (nH)	R_G (Ω)	R_D (Ω)	R_S (Ω)	C_{GDP} (fF)	C_{DSP} (fF)	C_{GSP} (fF)
35.6	15.0	1.5	1.1	16.38	9.18	4.29	21.40	22.10

Table 2 Summary of intrinsic parameters (V_{GS} = 0.5 V, V_{DS} = 1.5 V) for a 1.0x50 um^2 – $In_{0.25}Al_{0.75}As/In_{0.25}Ga_{0.75}As$ MODFET

C_{GS} (fF)	C_{GD} (fF)	C_{DS} (fF)	Rp (Ω)	R_i (Ω)	g_m (S)	g_{ds} (S)	τ (psec)
138.19	1.01	38.20	60.70	9.42	2.40E-02	5.41E-04	2.15

The unity current gain frequency (f_T), a common figure of merit, is 27 GHz based on our measurement results. In summary, the device demonstrates good performance despite the buried p-layer underneath the FET. Parasitic capacitance is fairly small because of the separation of p-layer to the modulation-doped channel.

3.2.2 PIN diodes

The pin structures were modeled with inductance and capacitance associated with the microwave pads and the common representation of a PIN diode shown in Figure 16. Table 3 lists the extracted parameters for two types of modulator structures. The M50A is an approximately 50x50 μm^2 pin structure whereas the M22B is a much smaller 22x22 μm^2 structure. In general, for the pin structures, the depletion capacitance scaled

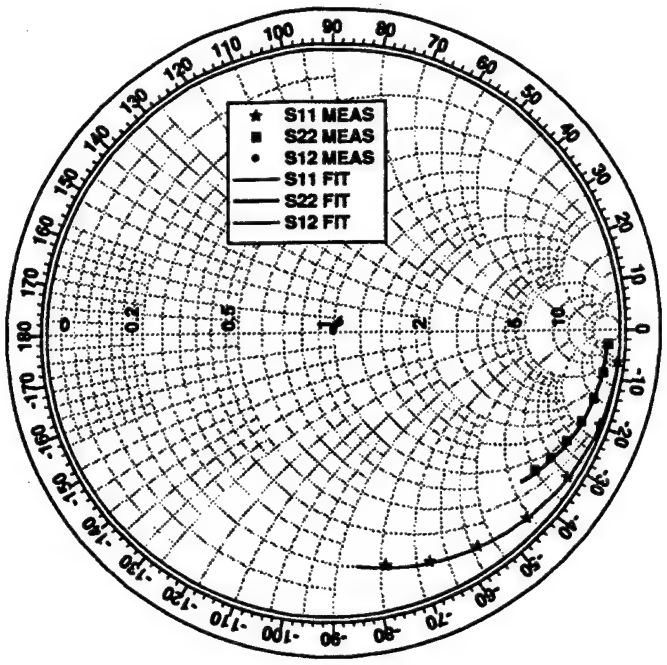


Figure 15 s11 and s22 smith chart of MODFET (measurements and data fitting)

directly with area. Also, the series resistance for the pin structures increased as the device size shrank due to the decreasing ohmic contact areas. However, in this particular case the M22B was a device that was entirely surrounded by the p-contact, whereas the M50A only had 3 sides of the mesa that had contact to the p-ohmic.

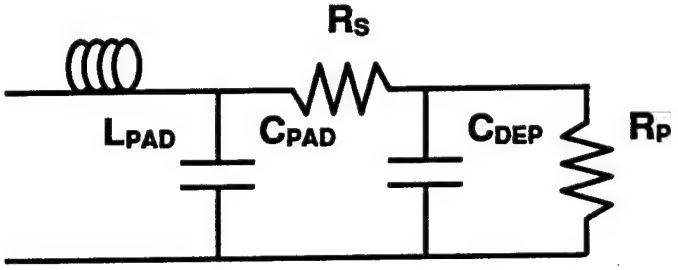


Figure 16 Equivalent circuit representation of a PIN diode

Table 3 Model parameters for two types of photodiode structures

	L_{PD} (nH)	C_{PD} (fF)	R_S (Ω)	C_{DEP} (fF)	R_P (Ω)
M50A	21.8	22.4	41.8	438.4	11386
M22B	21.1	21.0	35.4	88.0	26152

The 3-dB bandwidth, f_{-3dB}, is calculated from R_S and C_{DEP} with the influence of the large microwave pad parasitics. The reduction of the depletion capacitance by scaling

the devices to smaller dimensions increased the bandwidth significantly. Also, from the graph one can observe also the large effects of series resistance on the bandwidth. Two sets of data from two different samples are shown in the figure below (Figure 17) where R_S varied by a factor of two. This effect was primarily due to the series resistance from the p layer and p ohmic contact dominating R_S.

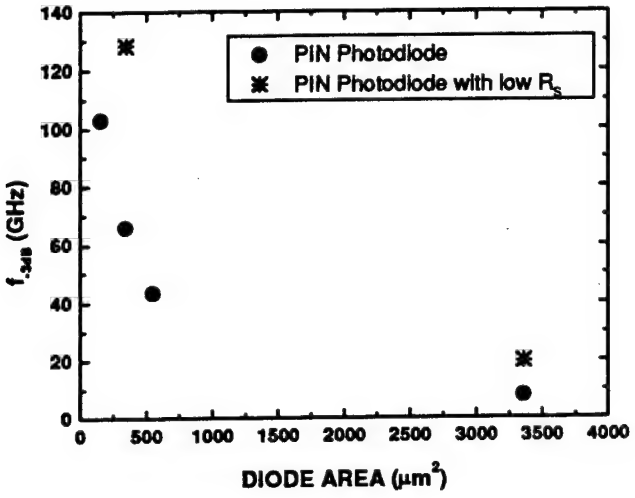


Figure 17 3-dB bandwidth versus photodiode area from various fabricated diode structures

3.3 Transimpedance receiver

The receiver circuit was based on a transimpedance design shown in Figure 18. The first stage is a transimpedance stage with a common source stage buffered by a source follower stage and a tunable FET providing resistive feedback to the input. This first stage provides conversion of the photocurrent generated in the photodiode into a voltage that is amplified by the preceding common-source stage. The outputs is taken after two more source follower stages which level shift and reduce the output voltage so that a 50-ohm output can be easily driven. Note the distinction between enhancement mode devices (black) and depletion mode devices (shaded).

Varying the feedback resistance (via V_{FB}) affects the transimpedance of the circuit as well as the bandwidth. Below is a graph (Figure 19) illustrating the effects of various feedback resistances on the output characteristics of the transimpedance stage with the larger resistance allowing for less required optical power. Figure 20 shows the closed transfer characteristics of the circuit measured under the DC conditions. The resistance is estimated from scaling a larger depletion device of the few working devices on the sample next to the receiver. Differences between the response of the simulated and measured circuits lies in the fact that the fabrication results varied from sample to sample and in between processing steps. The device characteristics were much different than average devices. The average depletion devices measured had a $g_m \sim 210$mS/mm. An overetch on the depletion mode devices resulted in a threshold that was near –0.5 V much

more enhancement than previous devices. Furthermore, the circuits were biased at V_{DD} =2.0 V because of concerns about the lower breakdown property of the FETs.

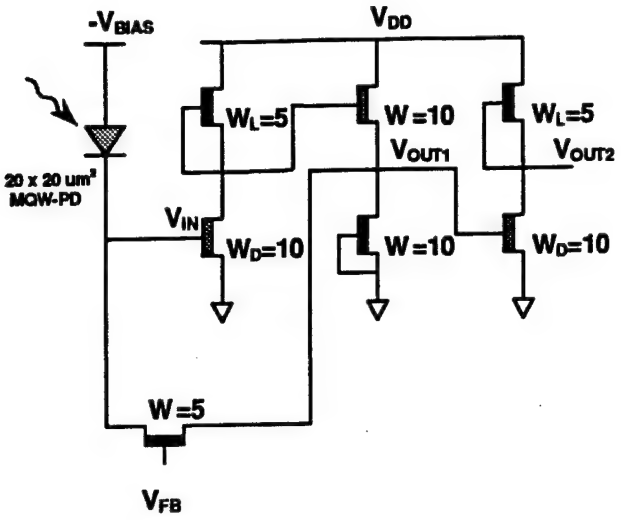


Figure 18 Transimpedance receiver circuit

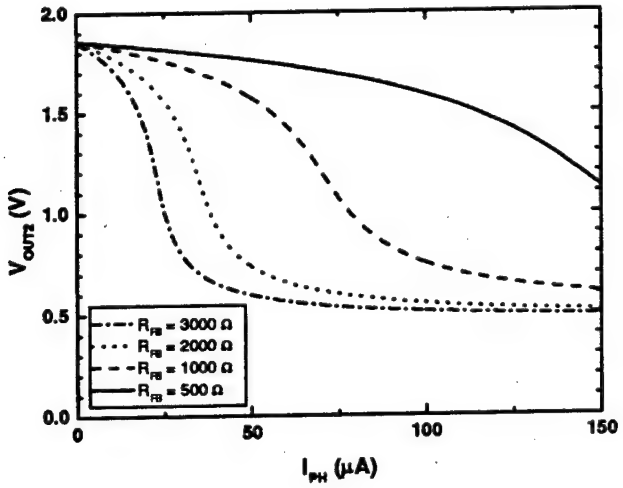


Figure 19 Simulated closed loop characteristics of the receiver circuit for various feedback resistances

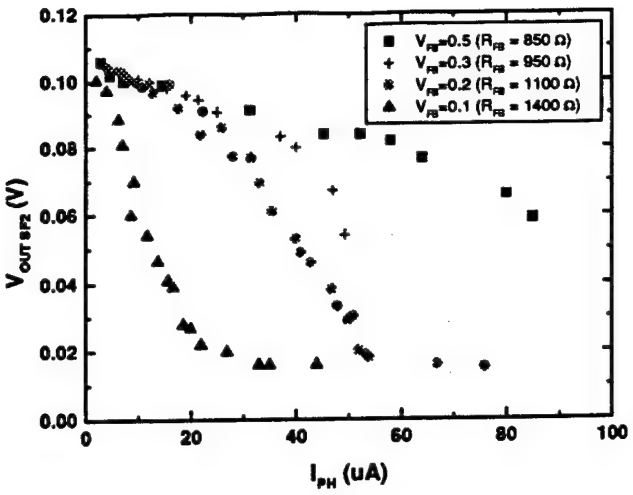


Figure 20 Measured closed loop characteristics of the receiver circuit

The high-frequency performance of the receiver is measured using a digital laser source at 850nm. This laser module was driven by an HP high-frequency digital source which had a bandwidth of 3 GHz. The receiver output was fairly constant till 1 GHz where the measured output signal started to shrink significantly. This happened for all the feedback VfB indicating the limiting bandwidth was that of the laser diode driver which was actually specified up to 500MHz. However, the output would follow the input modulation up to 2.5 GHz despite the shrinking waveform. Figure 21 is the transient response of the receiver at 1 GHz.

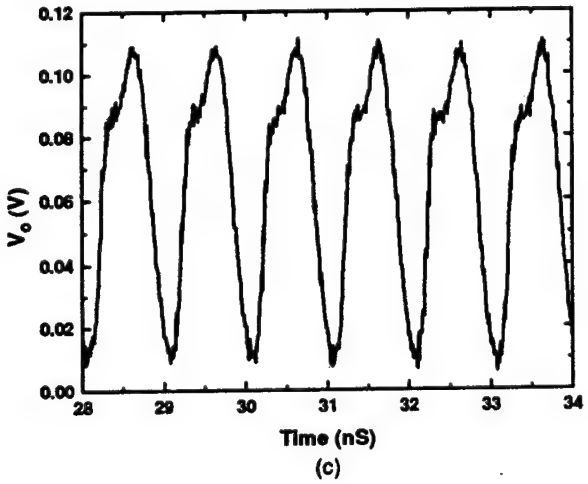


Figure 21 Receiver circuit transient response at 1 GHz

To estimate the bandwidth of the transimpedance receiver, we used the extracted device parameters and the analytic formula of the transfer function

$$H(\omega) \approx \frac{-R_F}{\left(1 + j\omega R_F\left(\frac{C_D + C_{IN}}{A} + C_F\right)\right)}. \qquad (11)$$

The corresponding equivalent circuit shown in Figure 22 was used to extract device parameters. The large dc gain, $A \sim g_m/g_o$, of the common-source circuit is approximately 30 to 40 primarily because of the low output conductance of these MODFETs. The input capacitance, C_{IN}, of the common source amplifier in the transimpedance stage is estimated to be about 60fF from the gate source capacitance and the miller effect capacitance. The photodiode depletion capacitance, C_D, for a $20x20\mu m^2$ device is approximately 80fF. The feedback capacitance is dependent on the drain-source capacitance of the tunable 5μm MODFET which is approximately 4.3fF. Thus, for a transimpedance (feedback resistance) in the low kilo-ohm range the bandwidth would be in the 5 to 9 GHz range.

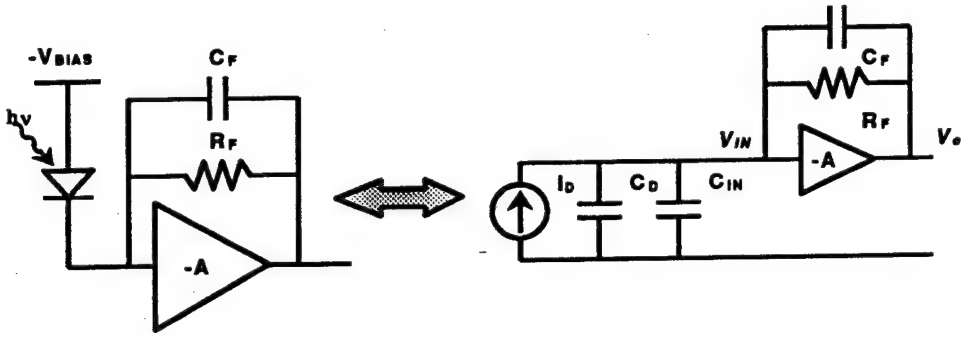
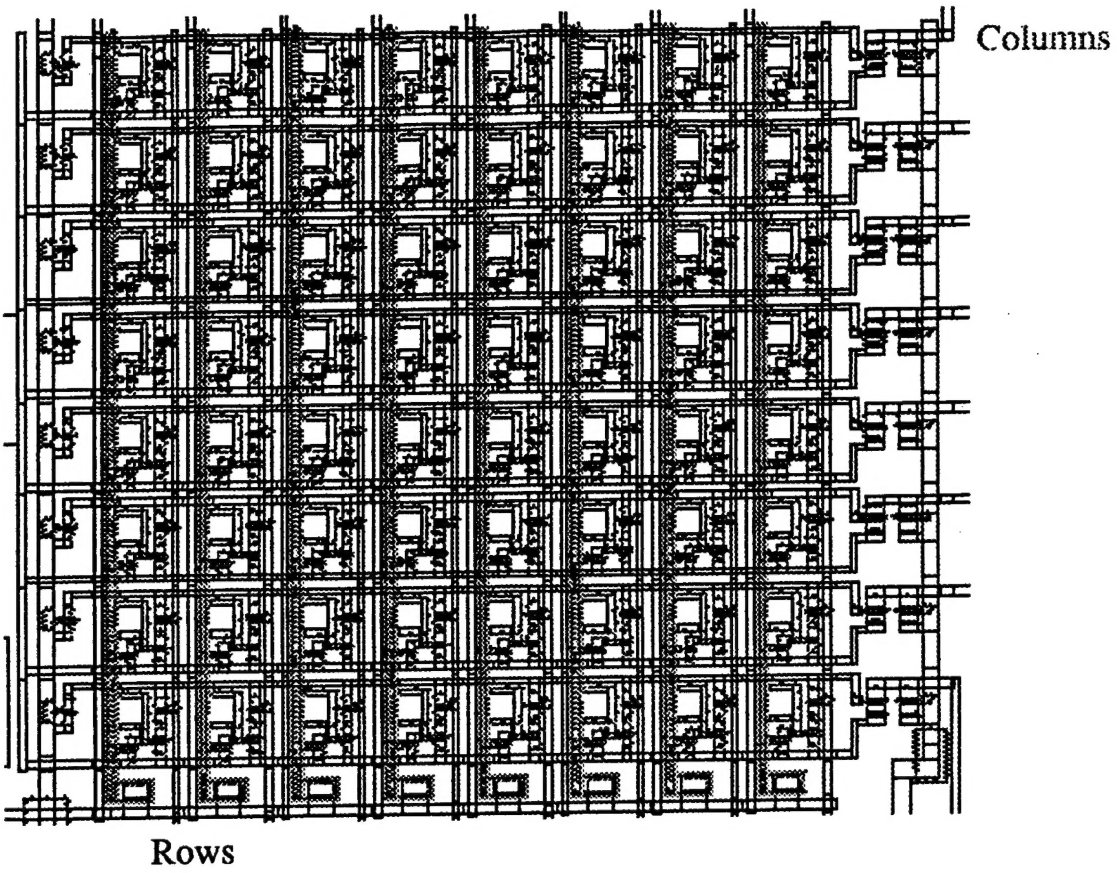


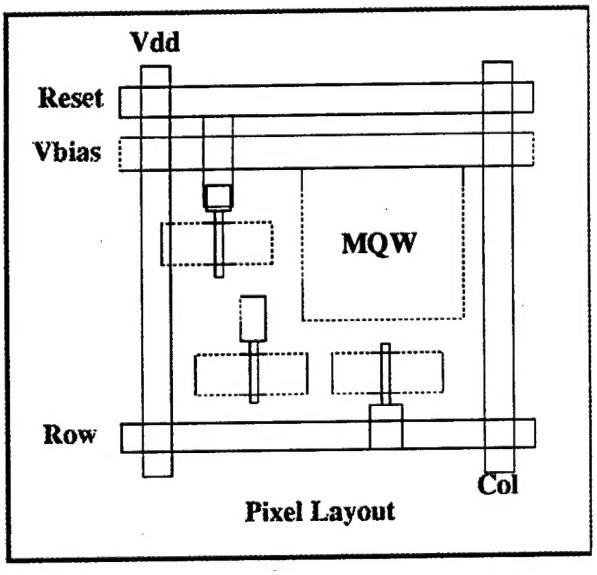
Figure 22 Equivalent circuit representation of a transimpedance amplifier

3.4 Active-pixel sensor array

With the monolithic integration technology, we also designed, fabricated and tested 8x8 active-pixel sensor (APS) arrays (Figure 23), with each pixel containing one MQW detector and three depletion-mode MODFETs. The array is controlled by an eight-stage shift register (Figure 24), so that rows can be read and reset sequentially. The pixel size is around 50 μm x 50 μm with a fill factor of 15%. Large APS arrays in GaAs can be used to perform the multiplexing of low-speed, highly parallel optical inputs onto a few high-speed electrical lines. The MQW/MODFET process offers the potential for very high-speed operation; as shown with the experimental results at 285 MHz (Figure 25), due to the large bandwidth FET devices and the low-capacitance, high-efficiency MQW detectors, as compared to standard Silicon CMOS designs. These results show potential for frame rates of up to several 100 of kHz on array sizes of up to 256x256.



(a)



(b)

Figure 23 (a) 8x8 active-pixel sensor layout, (b) individual pixels.

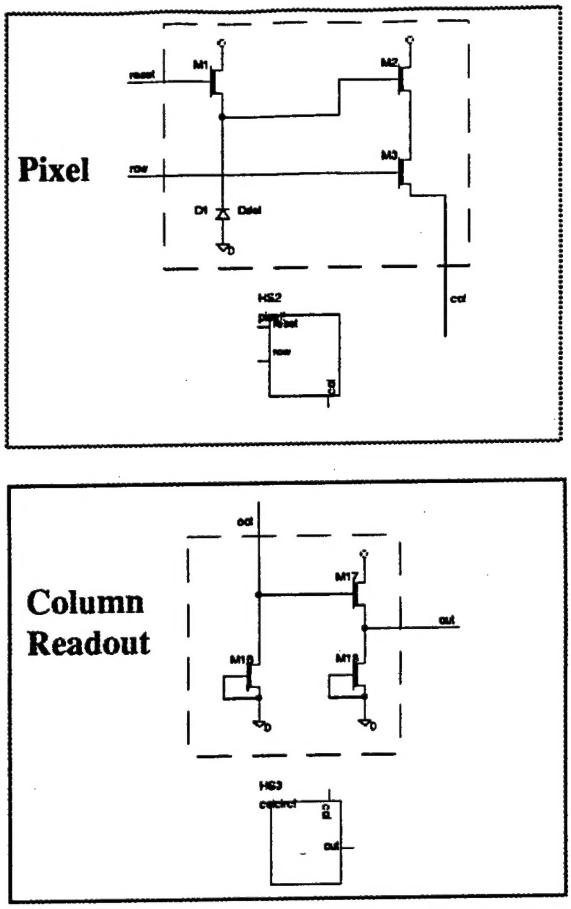


Figure 24 Circuit schematics of APS pixel and the readout

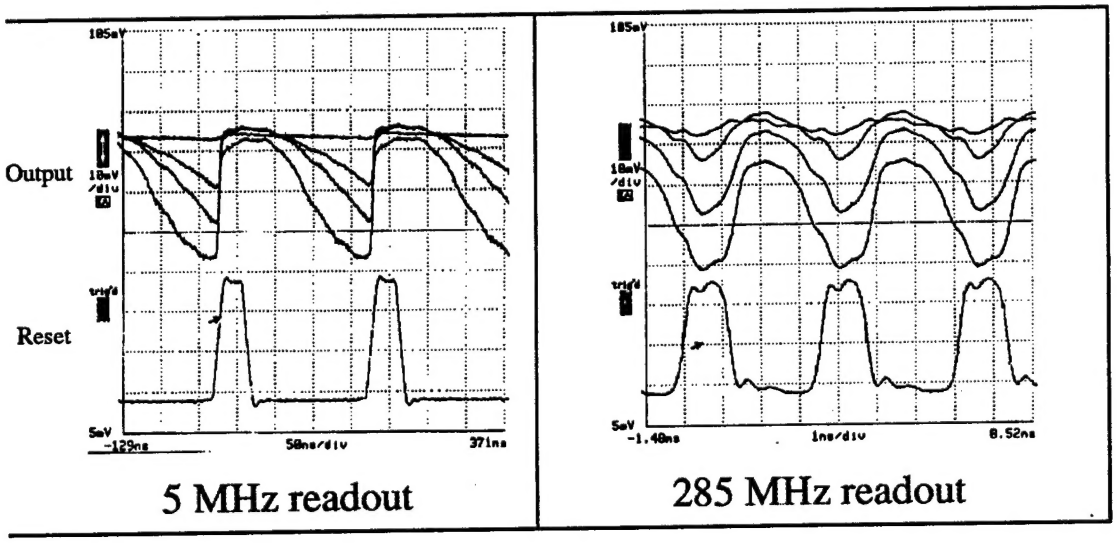


Figure 25 Experimental results from APS measurements

4. Summary

In this program, we have carried out an evaluation of optical transmitter and receiver technologies for parallel data processing applications. The system performances have been measured in term of the maximum interconnect density at a given data rate. The performance of two transmitter technologies, VCSELs and MQW modulators and their associated driver-receiver circuits including CMOS and bipolar transmitter driver circuits, and PN photodetectors with multistage transimpedance receiver circuits have been examined. At high bit rates (> 800 Mbits/sec), optimized links based on VCSELs and MQW modulators are comparable in terms of power dissipation. At low bit rates, the VCSEL threshold power dominates. The transmitter driver circuit is an important component in a link design, and it dissipates about the same amount of power as that of the transmitter itself. Scaling the CMOS technology from 0.5 μm down to 0.1 μm brings a 50% improvement in the maximum operating bit rate, which is around 4 Gbits/sec with 0.1 μm CMOS driver and receiver circuits. Transmitter driver circuits implemented with bipolar technology support a much higher operating bandwidth than CMOS technology; they dissipate, however, about twice the electrical power. An aggregate bandwidth in excess of 1 Tbits/sec-cm^2 can be achieved in an optimized free-space optical interconnect system using either VCSELs or MQW modulators as its transmitters.

A complete characterization of an optoelectronic monolithic technology have been carried out in this program. RF performance of the typical devices fabricated by the technology have been evaluated based on the s-parameter extraction from the devices. The bandwidth of the devices is around 9 GHz. We have fabricated a transimpemdance receiver circuit using the technology. The measured receiver bandwidth is 2.5 GHz limited by the transmitter bandwidth. A 8x8 active-pixel sensor arrays was also fabricated using the technology. A 285 MHz operation has been achieved experimentally, which indicates a potential for frame rates of up to several 100 of kHz on array sizes of up to 256x256.

5. *Related publications*

C. Fan, B. Mansoorian, D. A. Van Blerkom, M. W. Hansen, V. H. Ozguz, S. C. Esener, and G. C. Marsden, "Digital free-space optical interconnections: A comparison of transmitter technologies," *Applied Optics,* **34** (17) 3103-3115, June, 1995.

C. Fan, D. A. Van Blerkom, W. L. Hendrick, and S. C. Esener, "Free-Space Optical Interconnection: A Technology Comparison," *International Topical Meeting on Optical Computing,* Sendai, Japan, April, 1996.

C. Fan, D. A. Van Blerkom, W. L. Hendrick, and S. C. Esener, "Free-space optical interconnection: A technology comparison of vertical-cavity surface-emitting lasers and multiple-quantum-well modulators," *Optical Review,* **3**, 394-396, 1996.

C. Fan, D. A. Van Blerkom, and S. C. Esener, "Optimization of transmitter and receiver design for optoelectronic computing," *Digest IEEE/LEOS 1996 Summer Topical Meetings*, 72-73, 1996.

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D. A. Van Blerkom, O. Kibar, C. Fan, P. J. Marchand, and S. C. Esener, "VCSELs vs. MQW modulators for smart pixels from a link optimization perspective," *Technical Digest on OSA Topical Meeting on Spatial Light Modulators,* Lake Tahoe, NV, March 1997.

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C. Fan, B. Mansoorian, D. A. Van Blerkom, M. W. Hansen, V. H. Ozguz, S. C. Esener, and G. C. Marsden, "Digital free-space optical interconnections: A comparison of transmitter technologies," book chapter, *Optical Interconnects and Packaging,* SPIE Optical Engineering Press, 1998.